REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the Office Action mailed 11/28/05, Applicant is filing an RCE with this response. Claims 1-6, 9-16, 19 and 20 are no longer pending with the entering of new claims 21-28.

In the Office Action mailed 11/28/05, the Examiner has rejected claim 20 under 35 U.S.C. §101 as being directed to non-statutory subject matter. Applicant has canceled claim 20. Accordingly, Applicant requests the Examiner to withdraw the 35 U.S.C. §101 rejection.

In the latest office action, the Examiner has maintained the rejection of claims 1, 3-5, 11 and 13-15 under 35 U.S.C. §102(b) as being anticipated by Avnon et al. (U.S. Patent 5,559,977; "Avnon") and also has maintained the rejection under 35 U.S.C. §103(a) for the remaining pending claims. Specifically, claims 2, 9, 10, 12 and 19 as being unpatentable over Avnon in view of Patterson and Hennessy ("Computer Architecture A Quantitative Approach") and claims 6 and 16 over Avnon in view of Halfill ("SiByte Reveals 64-Bit Core for NPUs").

In reply, Applicant has submitted new claims 21-28. New independent claim 21 now recites a control circuit to inhibit co-issuance of an integer instruction to an integer pipeline when the integer instruction is subsequent to a first floating-point instruction in program order, until the first floating point-instruction reaches a stage in the floating-point pipeline where exceptions are to be generated. This is done to ensure that the integer instruction does not graduate from the integer pipeline prior to exception determination for the first floating point instruction in the floating-point pipeline.

Claim 21 also recites the control circuit to also inhibit co-issuance of a second floating-point instruction that follows the first floating-point instruction in program order, if the first floating-point instruction is not a short latency floating-point instruction. This is also done to ensure that the second floating-point instruction does not graduate prior to the exception determination for the first floating point instruction. However, the second floating-point instruction is not inhibited from co-issuance if the first floating-point

instruction is a short latency floating-point instruction, since in this instance, the second floating-point instruction will not graduate prior to the exception determination for the first floating-point instruction.

Independent claim 25 is a method claim which recites the actions performed as recited in claim 21.

Applicant submits that Avnon may teach integer and floating pipelines, in which stalls occur when floating-point instructions are determined to be unsafe. However, Avnon does not disclose the differentiation between short latency floating-point instructions and other floating-point instructions having longer latency. As stated in claims 21 and 25, co-issuance of a second floating-point instruction that follows the first floating-point instruction in program order is inhibited, if the first floating-point instruction is not a short latency floating-point instruction, but not inhibited from co-issuance if the first floating-point instruction is a short latency floating-point instruction. The embodiments of the invention, as now stated in the new claims, are not disclosed in Avnon or in any of the other relied upon references.

Accordingly, with the presentation of new claims, Applicant respectfully requests the Examiner to withdraw the previous 35 U.S.C. §102(b) and 35 U.S.C. §103(a) rejections. Furthermore, Applicant solicits for the allowance of new claims 21-28.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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